REMARKS

Claim 1 was rejected as anticipated by Renner. It is respectfully submitted that at least the following elements set forth in the claim are not found in Renner: an output processor that processes output signals from the digital signal processor and a storage selectively accessible by each of the processors.

The office action indicates that Renner teaches an element 20a which is an output processor. It is suggested that the element 20a is a processor which processes output signals from the digital signal processor.

The digital signal processor is indicated to be in a previous office action to include the combination of a multiply and accumulate processor, an input processor, an output processor, a master processor, and a storage including an external ROM, all as set forth in paragraph 3 of the office action mailed February 8, 2005. Thus, the outputs that are referred to in connection with an output processor that processes output signals "from the digital signal processor" must output from that combination of elements.

The element 20a is shown in Figure 1. It has the connections indicated in the office action, namely, a control connection 18 which only receives control signals and a parameter connection which only receives parameters, as indicated in Figure 1. The only output from the element 20a is to its data memory 34a. The element 20a is called a vector address generator. See column 3, line 30. The vector address generator 20a is operable to process instructions and generate addresses for output to associated data memories34. See column 3, lines 38-40.

Thus, all the vector address generators do is generate addresses for memories which are internal to the digital signal processor. They have nothing to do with processing output signals from the digital signal processor. The asserted output signals, in the form of elements 18 and 26, are both inputs to the element 20a, as clearly shown in Figure 1. The outputs are indicated as coming from the elements 12 and 24. But if the outputs come from the element 24, which is the array controller, then how in the world can it be said that the element 20a is the output processor?

Similarly, it is asserted that outputs come from the element 24, but the element 24 is the slave data processor. If those are the things that provide the outputs, then the element 20a has nothing to do with the outputs. Moreover, if these signals are received from internal

components, and are provided to internal components, it is clear that the element 20a has nothing to do with providing signals that are output from the digital signal processor. They simply do processing of address generation and have nothing to do with output processing. Therefore, there is no reasonable way to call the element 20a an output processor.

In addition, there is no storage selectively accessible by each of the processors that are set forth in the claim. It is suggested in the final rejection that each processor has a ROM "either internal or external to the processors, for element 12." See Final Rejection, paragraph 11. This sentence is internally inconsistent. Either the processors have a ROM or they do not. If they have a ROM, that ROM should not be associated with the element 12, the ROM should be associated with each of the processors to meet claim 1. The argument may be that the microcode 14, or if substituted for the microcode 14 storage, an external ROM may be used by the array controller. But, even if the array controller has its own accessible storage, there is nothing to indicate that such storage is accessible by any of the other processors, as required by claim 1. Column 3, lines 23-26 clearly says the ACS 12 has a ROM resident storage, but this does not mean any of the other elements, other than the ACS, have such a storage. Claim 1 calls for a storage selectively accessible by each of the processors, those processors being the mathematical processor, the input processor, the output processor, and a master processor. The ACS 12 cannot constitute all those processors and no office action to date has ever asserted such a position.

Also cited is column 8 which refers to an instructional ROM 176. There is supposed to be, according to the claim, a storage that is selectively accessible by each of the processors. The ROM 176 is internal to the vector address generators 20 and could not be accessible by each of them. Therefore, the assertion that the claim could read on the instruction ROM 176 described in column 8 makes no sense. Similarly, the assertion that column 9, lines 45-58, somehow supports the rejection is equally inapposite. There, there is a description of a ROM 40 which is asserted to be "not shown." The ROM 40 is a microcontrol store. See Figure 1. There is no indication that this microcontrol store is accessible by anything other than the slave data processor. There is no reason to believe that it is accessible by all the asserted processors.

Finally, column 3, lines 50-57, is cited. This includes a discussion of the array processor 12. It does not talk about any type of memory which is accessible to all the enumerated processors.

Finally, it is asserted without support that all of the ROMs for each processor, together, comprise the claimed storage selectively accessible by each of the processors. The problem with this argument is that each of the ROMs are only accessible by one processor. The claim calls for "a storage" that is selectively accessible "by each of the processors." There is no storage that each of the processors can selectively access. Instead, the Examiner is asserting that there are numerous storages which can be only accessed by one processor in each case. The claim language is clear that there must be "a storage" that is selectively accessible "by each of said processors." There is no one storage that each of the processors can access. That interpretation of the claim, which suggests that having a storage for each processor instead of a storage accessible by each processor, is unreasonable and is unsupportable. Therefore, reconsideration is respectfully requested.

On the same basis, reconsideration of the rejection of claim 16 is respectfully requested.

Respectfully submitted,

Date: July 14, 2005

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation